Amendments to the Claims:

Listing of Claims:

Claim 1 (currently amended) A semiconductor wafer comprising:

a ~~silicon~~ substrate with a first region, a second region, and a third region horizontally defined on [[a]] the surface thereof ~~of the substrate, the third region being adjacent to the first region and the second region~~; and

a capacitor disposed on the substrate, the capacitor further comprising:

a first electrode disposed in the first region and the third region on ~~the surface of~~ the ~~silicon~~ substrate;

a first isolation layer ~~covering~~ disposed on the first electrode ~~and the silicon substrate~~, the first isolation layer covering a portion of the first electrode and the substrate; and

a second electrode disposed ~~in the second region and the third region on the surface of the isolation layer~~ on the first isolation layer, the second electrode covering the first electrode in the third region and covering the substrate in the second region.

Claim 2 (currently amended) The semiconductor wafer of claim 1 wherein the capacitor further comprises a second isolation layer covering the capacitor and the ~~silicon~~ substrate.

Claim 3 (original) The semiconductor wafer of claim 2 wherein the capacitor further comprises a first contact plug located in the second isolation layer and electrically connected to the first electrode.

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Claim 4 (original) The semiconductor wafer of claim 3 wherein the first contact plug is located in the first region.

Claim 5 (original) The semiconductor wafer of claim 2 wherein the capacitor further comprises a second contact plug located in the second isolation layer and electrically connected to the second electrode.

Claim 6 (original) The semiconductor wafer of claim 5 wherein the second contact plug is located in the second region or the third region.

Claim 7 (original) The semiconductor wafer of claim 1 wherein the semiconductor wafer further comprises a field oxide layer located beneath the first electrode.

Claim 8 (original) The semiconductor wafer of claim 1 wherein the first electrode comprises a polysilicon layer or a doped polysilicon layer.

Claim 9 (original) The semiconductor wafer of claim 1 wherein the second electrode comprises a polysilicon layer or a doped polysilicon layer.

Claim 10 (original) The semiconductor wafer of claim 1 wherein the first isolation layer comprises a silicon oxide layer or a silicon nitride layer.

Claim 11 (currently amended) A capacitor disposed on a ~~silicon~~ substrate, the ~~silicon~~ substrate [[with]] having a first region, a second region, and a third region horizontally defined on [[a]] the surface ~~of the silicon substrate~~ thereof, ~~the third region being adjacent to the first region and the~~

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~~second region~~, the capacitor comprising:

a first polysilicon layer disposed in the first region and the third region on the ~~surface of the silicon~~ substrate;

a dielectric layer covering a portion of the first polysilicon layer and the ~~silicon~~ substrate; and

a second polysilicon layer disposed ~~in the second region and the third region on the surface of the dielectric layer~~ on the dielectric layer, the second polysilicon layer covering the first polysilicon layer in the third region and covering the substrate in the second region.

Claim 12 (original) The capacitor of claim 11 wherein the capacitor further comprises a first contact plug electrically connected to the first polysilicon layer.

Claim 13 (original) The capacitor of claim 12 wherein the first contact plug is located in the first region.

Claim 14 (original) The capacitor of claim 11 wherein the capacitor further comprises a second contact plug electrically connected to the second polysilicon layer.

Claim 15 (original) The capacitor of claim 14 wherein the second contact plug is located in the second region or the third region.

Claim 16 (original) The capacitor of claim 11 wherein the capacitor further comprises a field oxide layer located under the first polysilicon layer.

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